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LOW-JITTER REFERENCE-BASED SYNCHRONIZATION FOR DUAL RF TRANSMITTERS

Purpose. To develop a low-jitter synchronization unit for two radio transmitters based on a com-mon reference oscillator in 0.18 μm CMOS technology.

Methodology. The work utilizes circuit simulation methods in the MATLAB/Simulink environment using the bilinear z-transform to analyze the dynamics of Phase-Locked Loop (PLL) stages. The PCB layout design was carried out considering electrodynamic parameters (a target impedance of 50 ohms and FR-4 material) alongside RC parameter extraction to minimize phase skew. Experimental verification was conducted based on 0.18 μm CMOS technology.

Findings. A dual-loop architecture (consisting of a Clock and Data Recovery (CDR) block and a jitter filter) was created, ensuring signal stability at a frequency of 1.173 GHz. A phase noise level of -101.52 dBc/Hz at a 100 kHz offset and a root mean square (RMS) jitter of 3.3 ps for the synthesizer and 4.2 ps for the CDR node were achieved. The frequency lock time is 27.3 microseconds with a power consumption of 36 mW per node.

Originality. The use of an innovative charge pump architecture with an operational error amplifier is justified for precise potential equalization of nodes, which minimizes parasitic spurs and phase shift. For the first time, the integration of OR logic directly into the structure of the prescaler's D-flip-flops has been proposed, eliminating additional signal propagation delays and reducing cumulative jitter.

Practical value. The proposed solution allows for the abandonment of complex software-based phase skew correction algorithms in Massive MIMO and SDR systems. The low jitter level (3.3 ps) enables the stable deployment of higher-order quadrature modulation schemes, including 256 QAM, thereby improving the error vector magnitude (EVM) and the efficiency of next-generation radio links.

Keywords: *phase coherence, jitter, PLL, CDR, TCXO, prescaler, synchronization, beamforming*

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Introduction. In modern high-speed radiophysical systems and distributed antenna arrays, phase coherence is not just an auxiliary parameter, but has become the basis for systematic determinism in phase relationships. In massive MIMO systems and full-duplex transceivers, the requirement for synchronization is critical to the effective use of spatial channel multiplexing. The absence of transceiver coherence leads to phase drift, which deterministically shifts the spatial nulls in the radiation pattern. In full-duplex transceivers, the absence of phase coherence prevents the effective use of self-interference cancellation (SIC), since the phase difference between the cancellation vector and the leakage vector of the local transmitter immediately affects the dynamic range of the receiver path. The elimination of plesiochronous operation and the use of a single time base have thus become critical to the realization of the theoretically derived beamforming efficiency and the prevention of degradation in the signal-to-noise ratio [1]. The system's performance in this context is critically limited by the quality of the time base, and thus requires precise analysis of the phase distortions at the physical level.

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The physical basis of signal vector accuracy distortion, or EVM, in wideband communication systems is intrinsically related to the spectral density of phase noise and the integrated jitter of the synthesizer. With 0.18 μm CMOS technology, it has been proven that achieving a phase noise level of –101.52 dBc/Hz at an offset of 100 kHz and an RMS jitter of 3.3 ps is a significant problem, requiring the inclusion of an improved current matching charge pump, etc. [2]. With regard to the vector analysis of the problem, it is evident that the presence of phase noise leads to a constricting effect on the decision space for high-order QAM modulations. The problem of jitter in PLL-based synthesizers is critical with regard to the maintenance of low BER levels. Any variation in the reference signal in one of the paths inevitably leads to mutual timing misalignment in multichannel architectures. The strategic importance of the problem of timing alignment of digital streams in a network of distributed nodes is related to the need for compensating for timing skew caused by ISI and bandwidth constraints of the channel. Data-dependent jitter introduces uncertainty in data recovery operations, with peak distortions reaching 150 ps. Quarter rate architectures are necessary to counter these effects and ensure stable sampling. Such architectures ensure orthogonal phases,

which is critical for the correct functioning of rotary frequency detectors [3]. Such architectures ensure the recovery of the clock signal with an accuracy of 4.2 ps (RMS) even with the presence of distortions on the input signal of approximately 150 ps (p-p) and ensure the synchronicity of nodes in the network with high data densities. Temporal stability is intrinsically related to the stability of the reference signal and the conversion characteristics.

In the context of precision data acquisition systems, the instabilities inherent in the reference oscillator would adversely affect the precision of the analog-to-digital converters. The jitter effect on the reference signal would cause aperture uncertainty, resulting in the generation of spurious components. This would not only impose restrictions on the spurious-free dynamic range but would also compromise the timing accuracy of the events within the coherent network. In the case of plesiochronous nodes, the inherent use of separate oscillators would cause the accumulation of phase error, thus resulting in the occurrence of overflow, which would prevent the correct comparison of data from different sensors. This degradation further supports the proposition that the use of different frequency sources is not desirable for large-scale synchronous systems. The major technological challenge in the design of coherent arrays lies in the establishment of a single "point of truth" for the phase and frequency for the entire distributed system. The challenge arises from the requirement to minimize the additional jitter that inevitably accumulates in the signal distribution lines. The design methodology for the coherent array is to use a two-loop architecture. In the proposed design, the first loop would be for the frequency acquisition and clock recovery, implemented by the CDR. The second loop would consist of a narrowband jitter filter and a high-Q LC-based oscillator, denoted by LC-VCO. This design methodology would be effective in eliminating the accumulation of phase within the distribution network, thus ensuring the desired purity for the reference signal to enable the correct operation of the high-speed interfaces and the precision RF paths within the single phase-locked domain.

Literature review. In modern microelectronics, the development of high-speed interfaces involves a critical investigation of jitter transfer functions. The minimization of timing uncertainties is a strategic requirement to ensure the integrity of signals in gigabit networks. The 8B/10B coding scheme is a major component in this context, not only ensuring the density requirements for the detectors but also providing DC balance, an essential requirement for AC-coupled connections [1].

Clock and data recovery (CDR) systems play a crucial role in the mitigation of phase skew between the clock and data signals. The development of PLL structures based on monolithic integrated circuits (MICs) allows for invariance to process variations and temperature changes by matching components to precise values on a single chip [3]. Differential signaling is used to obtain high noise immunity and to reject common noise in channels with small voltage amplitudes [4, 5].

The theoretical basis for designing such systems involves classical PLL models. In the steady state, the dynamics of the PLL are modeled by linear approximation in the S-domain [6]. This allows for the optimization of the trade-off between the loop bandwidth and the minimization of phase noise [7–9]. The data suggest a trend towards multi-loop structures, where the separation of frequency locking and phase wander filtering is a prerequisite for the achievement of sub-picosecond accuracy.

The shift towards a distributed architecture of local oscillators calls for a re-design of the traditional topology in favor of a solution that ensures the minimum accumulation of jitter. This is effectively achieved through two-loop architectures that combine a CDR loop with a narrowband jitter filter for the purification of the clock signal. The integration of phase-frequency detectors with dynamic logic architectures, like the TSPC, increases the acquisition range of the loop and removes the "kill zones", which is a requirement for precision systems.

The optimization of the power consumption of the distribution network is carried out through architectures that operate at lower clock rates (1/4-rate), allowing the implementation of PFD logic through a CMOS framework rather than the Current-Mode Logic (CML). The implementation of this topology at the physical layer is carried out through the integration of high-speed D flip-flops with OR logic, also known as dual modulus prescalers. This ensures the minimization of the topology. An LC-VCO is used as the oscillator in the circuit. The oscillator is designed using the RF CMOS process. In order to avoid the degradation of the Q factor of the circuit through the integration of cross-coupled amplifiers, noise filtering is carried out through the integration of resonant circuits L2, C2, L3, C3 operating at twice the frequency.

Comparative characteristics of architectural solutions.

The 1/4-rate architecture is identified as the most promising architecture for the design of multichannel systems, providing the optimal compromise between operating speed and efficiency. Moreover, it allows the utilization of standard cells of CMOS technology for the implementation of the digital phase processing.

The random jitter of the differential stages is related to the thermal noise. Mathematically, it is a function of the bias current Iss and the capacitive load CL. In practice, it has been observed that the additive jitter of the output driver (approximately 0.022 ps RMS) is often negligible when compared with the jitter of the PLL loop itself and the clock tree distribution circuits.

The channel bandwidth (f_media) constrains the deterministic jitter (DDJ/ISI). In this context, the peak

Table 1

Comparative analysis of clock distribution architectures

Type of architecture	Jitter minimization method	Area efficiency	Justification for use
Full-rate CDR	Direct phase locking	High	Moderate Speed Systems (CML Logic)
1/4-rate PFD	Multiphase sampling (16 phases)	Average	High-speed MMICs; transition from CML to CMOS [10]
Dual-loop	Cascade filtering	Low	Precision networks; ISI and phase noise suppression

Table 2

Matrix of influence of destabilizing factors

Factor	Physical nature	Influence on phase	Compensation method
CP current mismatch	NMOS/PMOS drain-source potential difference	Static phase error [11,12]	Self-centering cascode mirror and error amplifier
ISI/DDJ	Bandwidth limitation	Deterministic jitter	Equalizing and 8B/10B encoding (Ensure transitions)
Power supply noise	Power/Ground bounce	VCO frequency modulation	Differential buffers and decoupling of Mp/Mn nodes [12]

jitter is linearly related to the channel time constant \(\tau\) and the bit period T. This induces intersymbol interference, which distorts the eye diagram and the threshold crossing times.

Impedance inhomogeneities, which arise from the SMA connectors, vias, and bonding wires, induce reflections that contribute significantly to the phase instability.

Analysis of degradation factors.

The usage of operational amplifier configurations in the implementation of charge pump circuits for the purpose of equalizing the VX and VOUT node potentials, along with cascode structures, may help to mitigate the effects of charge sharing in a significant manner.

Problem statement. Ongoing developments in data acquisition systems, especially in particle physics experiments, make it necessary to abandon the plesiochronous mode, in which the frequency differences between the reference oscillators used in the system are compensated by the presence of elastic buffers. The presence of elastic buffers introduces unpredictable delays, which makes it difficult to achieve precise time stamping.

There is a need to balance the need for phase coherence across a number of nodes connected to a single source, which is located remotely, and the degradation of the signal in the distribution networks. Physical constraints, which include the presence of additive jitter at the nodes in the branching networks and the dynamic phase shifts, make it difficult to achieve the picosecond level stability. In order to overcome the difficulties associated with the implementation of the direct drive systems, it is necessary to develop methods for the compensation of the phase shifts. This requires the synthesis of adaptive PLL structures that may help to achieve RMS jitter values less than 4.2 ps in the presence of high ISI.

The purpose of the study is to develop a low-jitter synchronization unit for two radio transmitters based on a common reference oscillator in 0.18 μm CMOS technology.

To achieve this purpose, the following objectives were formulated:

1. To analyze dominant sources of phase noise and jitter accumulation in PLL-based multichannel architectures.

2. To develop a dual-loop architecture combining a CDR block with a narrowband LC-based jitter filter.

3. To design a dual-modulus prescaler with OR logic integrated directly into the D-flip-flop structure.

4. To implement a charge pump with an operational error amplifier for precise node potential equalization.

5. To develop a 50 Ω PCB layout with RC parasitic extraction to minimize inter-channel phase skew.

6. To experimentally verify the proposed architecture and validate key performance metrics in 0.18 μm CMOS technology.

In multichannel microwave system architectures, the temperature-compensated crystal oscillator plays a critical role as a fundamental element that defines the system-wide phase budget. The selection of a highly stable reference signal is not merely a matter of frequency accuracy; rather, it defines the "pedestal" level of phase noise, which will inevitably scale according to a 20 log(N) law, wherein N represents the frequency ratio, as defined by the phase-locked loop. For digital broadcast applications, the use of an external crystal oscillator [12] becomes a necessary requirement for long-term stability, as a means to minimize initial jitter and substrate noise, both of which are critical considerations for deep submicron CMOS technologies [13].

In the proposed system, the external 16.38 MHz oscillator drives the prescaler input with a division factor of 8, thereby generating the phase-locked frequency detector comparison frequency. The use of this approach strikes a balance between loop bandwidth and frequency settling speed, while maintaining a high level of timestamp accuracy for radio network applications [14]. As the temperature drift of a TCXO correlates directly with phase uncertainty, the use of temperature-compensated oscillators becomes a valid engineering compromise between cost and the ability to maintain a level of coherence without the requirement for continuous calibration [4]. The reference signal stability, as defined by the PFD input, establishes the lower limit for phase distortion, which is ultimately propagated through the clock distribution network [15].

Developing a Clock Distribution Architecture with Minimal Jitter.

The requirement of gigahertz-range signal distribution necessitates the use of precision frequency division circuits without the introduction of any additional phase delays. The core of the system is the RF PLL synthesizer built using the 0.18 μm CMOS process technology, with the critical block being the high-speed mixed signal down-scaling circuit [15]. The prescaler DMP is built as a dual-module architecture with 16/17 division using Source Coupled Logic (SCL) and True Single Phase Clock (TSPC) logic to ensure low power consumption [16]. Special emphasis is given to the D-type flip-flop design with the integration of OR logic to create the dual division module. This reduces the overall switching delay, increases the frequency operation, and greatly simplifies the crystal layout [17].

To ensure the optimization of power consumption with minimal electromagnetic interference to the analog circuits, the 1/4-rate architecture is chosen to reduce the operating frequency while maintaining the high operating frequency [18]. The measured intrinsic RMS jitter is 3.3 ps, validating the use of mixed-mode circuits to ensure the minimization of phase distortion [10]. This circuit design creates a coherent platform for physical

distribution at the PCB layout level with the integration of parasitic parameters.

In the physical design stage (back-end design), the dominant uncertainty factor is the phase skew between channels. In deep submicron design (DSM) circuits built using linear wire load models, the results do not meet the accuracy requirements, necessitating the use of special tools such as Synopsys Apollo [11]. The design process includes the use of RC parameter extraction with subsequent back-annotation to ensure the verification of timing delays with programmable dividers [12]. Any variations in the length of the traces or the pad capacitances can result in the degradation of coherence, necessitating the integration of the capacitive effects of electrostatic discharge (ESD) buffers into the layout design.

To maintain signal integrity and accurately measure the phase, 50-ohm buffers are integrated within the system to match the nodes with measurement equipment and reduce reflections on signal transmission paths [13]. The accuracy of parasitic parameter modeling in the post-layout stage directly impacts the final phase skew between transmitters. Systematic modeling of RC delays guarantees that timing uncertainties are within specified limits to meet beamforming and spatial coding algorithm requirements.

To realize an ideal level of phase coherence, a two-loop system structure is required: a 1/4-rate clock and data recovery loop to recover the clock from data and a clock jitter filter to purify it. Current imbalance in the charge pump contributes significantly to parasitic spurs in the spectrum. This problem is addressed by an innovative architecture that utilizes an operational error amplifier to equate potentials on the reference and output nodes to ensure precise current matching. The LC variable coil oscillator plays a major role in clock jitter suppression by providing a narrowband filter for the clock signal.

Jitter filter cascading enables effective suppression of phase noise from system components. In a system with bandwidth-constrained channels, a level of deterministic jitter caused by intersymbol interference is inevitable. With a maximum ISI amplitude of 150 ps peak-to-peak, the proposed clock jitter filter architecture maintains an output jitter of 4.2 ps RMS. This guarantees compliance with strict standards like SONET and maintains signal constellation stability. Thus, this proposed solution with a stable reference source, precise division via D-triggers with OR logic, and two-loop jitter filtering provides a technically complete solution to realize a phase-coherent radio system.

Materials and methods of research. ***Synchronization system architecture.*** In multichannel electronic systems, which exhibit sensitivity to phase distortion, the application of a centralized synchronization approach can be considered a fundamental strategy for addressing issues associated with inter-channel phase mismatch. The application of this approach ensures the establishment of a common time scale across all signal conversion stages, thereby eliminating the possibility of stochastic synchronization errors. The frequency source, which serves as the reference signal, is a temperature-compensated crystal oscillator. The output frequency, represented as f_crystal, is 16.38 MHz. To optimize power consumption and reduce the frequency of the CMOS logic, which is a component of the phase-locked loop, a divide-by-8 approach is applied, thereby reducing the frequency to 2.048 MHz, which is the comparison frequency of the phase detection detector [2].

The design addresses the application of a dual coherent RF signal approach. The application of a single temperature-compensated crystal oscillator, along with a clock signal distributed via a symmetric H-tree topology comprising a group of precision fan-out buffers, ensures the production of identical phase portraits for both local oscillators. The application of a 1/4 rate phase distribution approach ensures a wide loop acquisition range without the application of an external reference signal for data recovery, thereby addressing a critical requirement for the preservation of quadrature modulation accuracy and error vector magnitude, thus ensuring conformity with the intrinsic characteristics of the frequency source [3].

Reference frequency source. The strategic importance of the temperature-compensated crystal oscillator (TCXO) lies in its capability to provide stability over short- as well as long-term periods in the face of temperature changes. As opposed to the conventional crystal oscillators, the TCXO chosen here effectively filters the environmental changes, thereby reducing the effects of 1/f noise close to the carrier [4]. As far as the DVB-T system is concerned, the modulation accuracy is directly proportional to the integral jitter value, as the phase noise of the reference source defines the lower sensitivity of the receiver. As per the analysis of the jitter budget, it has been established that as the final value of the RMS jitter of the signal at 1.173 GHz is 3.3 ps, the contribution of the reference oscillator at 16.38 MHz is minimal, while the dominant values are those of the dividers as well as the phase detector [5]. The technical requirements of the reference source as well as the synthesized signal are presented in Table 3.

The chosen TCXO ensures sufficient stability for the 3-pole loop filter, which is effective in suppressing the VCO's phase noise and transitioning to signal distribution throughout the board.

Clock distribution network. To ensure signal integrity during distribution, it is imperative to minimize the additive jitter contributed by active network components. For this purpose, the PLL configuration uses a charge pump with an innovative technique for matching the currents, thus minimizing the phase shift and spurious

Table 3

Comparative characteristics and requirements for the frequency source

Parameter	Unit of measure	Meaning	Impact on the system
TCXO frequency (*fcrystal*)	MHz	16.38	Basic system stability [6]
PFD frequency (*fref*)	MHz	2.048	Mesh pitch and loop capture speed
Phase noise (100 kHz offset)	dBc/Hz	–101.52	Spectral purity of the carrier is 1.173 GHz
RMS jitter	ps	3.3	Increase in bit error rate (BER) [7]
Power consumption (PLL)	mW	36.0	Energy efficiency of 0.18 μm CMOS

tones [8]. Implementing 1/4-bit clock distribution facilitates a lower CMOS logic frequency, which significantly reduces the system's dynamic power consumption, which is as high as 170 mW for the entire CDR and jitter filter. For minimizing reflections on high-frequency lines, precise impedance matching is achieved, with mathematical verification through the calculation of reflection coefficients at branching nodes [9].

The overall root mean square jitter is calculated as the geometric sum of source jitter and additive network jitter, as represented by

$$\Delta t_{sys,rms} = \sqrt{\Delta t_{sys,rms} + \Delta t^2_{add,rms}},$$

where $\Delta t_{sys,\,rms}$ is a total system root mean square jitter; $\Delta t_{src,\,rms}$ is TCXO output-referred jitter; $\Delta t_{add,\,rms}$ is additive jitter introduced by buffers, dividers and charge pump circuits [10].

The integration of the rotary frequency detector into the CDR process eliminates the need for a local reference on the client side, thus extending the acquisition range [11]. This requires hardware delay compensation, and the latter is achieved on the printed circuit board (PCB) layout level.

Printed circuit board design. The PCB layout is critical for phase locking at the gigahertz level. A four-layer FR-4 stackup material is used, where $\in_r = 4.4$. In order to control the return currents and prevent electromagnetic interference, the Internal 1 and Bottom Layers are used as a solid ground plane and are connected via stitching [12]. The major requirement is to maintain a target impedance value of 50 Ω for single-ended traces and 100 Ω for differential traces, achieved by precise control over the width and prepreg thickness. The PCB layer specifications and the associated electrodynamic parameters are provided in Table 4.

The characteristic impedance of a microstrip line is calculated using the formula

$$Z_0 = \frac{87}{\sqrt{\in_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right),$$

where w is a conductor width; h is a dielectric thickness (200 μm); t is a copper thickness (35 μm); $\in_r$ is permittivity (4.4) [14].

Parameter estimation methodology:

1. System verification includes the measurement of phase noise and inter-channel skew. In order to test the spectral purity of the generated 1.173 GHz signal, the integration method of the phase noise density function $L(f)$ is used [15].

Table 4

Layer specification and electrodynamic parameters of PCB

Layer	Material	Thickness (μm)	Assignment/ Impedance
Top Layer	Copper (RF)	35	Signal/50 Ohm (w = 360 μm)
Dielectric 1	FR-4 ($\in_r$ = 4.4)	200	Insulation (Prepreg)
Internal 1	Copper (GND)	35	Screen/Support plane
Dielectric 2	FR-4	1,000	Foundation (Core)
Bottom Layer	Copper (Power/GND)	35	Power and shielding [13]

2. Relationship between phase noise and integrated jitter

$$\Delta t_{rms} = \frac{1}{2\pi f_c}\sqrt{2\int_{f_1}^{f_2} L(f)df},$$

where f_c =1.173 GHz, and the integration limits, f_1 = 10 kHz, f_2 = 10 MHz are determined by the requirements of the DVB-T standard [16].

3. Calculating the time shift (Time Skew)

$$\Delta t_{skew} = \frac{\Delta L\sqrt{\in_e ff}}{c}.$$

4. For a length difference of ΔL = 1 mm and $\in_{eff} \approx 3.3$, $\Delta t_{skew} \approx 6$ ps. For a frequency of 1.173 GHz, this corresponds to a phase error of $\Delta\Phi = 360 \times f_c \times \Delta t_{skew} \approx 2.5°$, which is acceptable for the selected modulation type [17].

5. Estimation of the total measurement error

$$\sigma_{total} = \sqrt{\sigma^2_{instr} + \sigma^2_{rand}}.$$

6. In the above expression, σ_{instr} refers to the instrumental error of the spectrum analyzer, whereas σ_{rand} represents the stochastic term [18]. Moreover, the RMS jitter of the filter output, when subjected to 150 ps of intersymbol interference (ISI) at the input, does not exceed 4.2 ps, thus validating the effectiveness of the proposed two-loop structure.

Results. Rationale for the Results of a Study on the Characteristics of Low-Jitter Frequency Synthesis and Synchronization Systems.

1. Analysis of timing responses and jitter measurement outcomes. In modern gigabit data networks, signal integrity requires precise control over the timing uncertainties associated with signal edges. In fact, excessive jitter has been shown to cause an exponentially increasing bit error rate (BER) [1]. The study reveals the crucial technological differentiators for the practical application of a unique Artisan 0.18-μm CMOS standard element library, along with an improved wire load model, which considers non-linear propagation delays along the signal propagation paths. The major architectural innovation was the integration of improved D-latch structures based on Source Coupled Logic (SCL) and OR logic within the master latch. This allows for the integration of two-module division operations, thus reducing propagation delays and minimizing cumulative noise in down-scaling operations. The device, implemented in 0.18-μm CMOS, was prototypically tested and confirmed to produce a root mean square (RMS) jitter of 3.3 ps for the phase-locked loop (PLL) [2]. In the clock and data recovery (CDR) device, the input jitter was 150 ps peak-to-peak, and the RMS jitter at the output was 4.2 ps. Significant attention was focused on reducing deterministic jitter (DDJ/ISI) caused by bandwidth limitations of the channel. The effectiveness of a two-loop configuration (front-end CDR, clock jitter filter) was verified. The addition of a rotary frequency detector in the first loop enhances the acquisition window in the absence of any reference signal, while the second loop, based on an LC oscillator, provides accurate filtering of

high-frequency variations. Quantitative time-domain parameters are correlated with spectral purity, thereby describing the frequency-domain characteristics of the system.

2. Spectral characteristics & phase noise analysis. Spectral purity is the basis of inter-channel interference mitigation. Phase noise of the system is significantly affected by the phase-frequency detector (PFD) architecture and parameters of the third-order loop filter. A phase noise level of –101.52 dBc/Hz was recorded at the synthesizer, operating at a 100 kHz offset from a 1.173 GHz carrier [7]. This low phase noise was achieved by using a noise filtering method in the voltage-controlled oscillator (VCO) by using resonant circuits (L2, C2 & L3, C3) at $2\omega_0$, thereby reducing Q-factor degradation caused by cross-coupled amplifiers.

A second-order model was used to analyze the jitter transfer function (JTF)

$$H_{closed}(2) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2},$$

where ζ is the damping coefficient; ω_n is the natural frequency of the loop; s is the complex Laplace variable [8]. The contribution of the VCO to the overall phase noise spectral density was estimated taking into account thermal noise and the $1/f_2$ region (Leeson model)

$$L\{\Delta\omega\} = 10 \times \log_{10}\left[\frac{2kT}{P_{sig}} \times \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right].$$

In this case, k stands for the Boltzmann constant; T is the temperature; P_{sig} is the signal power; Q is the quality factor of the circuit, while $\Delta\omega$ stands for the carrier offset frequency, also known as the Leeson frequency [9]. High spectral efficiency is directly related to the matching of currents in the charge pump, as it helps in minimizing phase shifts caused by parasitic spurs.

3. Interchannel phase difference and skew minimization. In multichannel systems, it is important to have phase identity between the channels in order to recover the data correctly [11]. The main method for reducing phase skew is based on the matching of charge and discharge currents in the charge pump [12]. The proposed architecture utilizes a high-gain error amplifier responsible for equalizing the potential of the V_X node and the VOUT node, thereby making the IUP and IDOWN currents equal. To reduce the effects of the "dead zone" of the phase-frequency detector, formed by the True Single Phase Clock (TSPC) logic, a delay element was added to the reset circuit. The parameters of the loop are presented in Table 5.

Hardware equalization of currents guarantees phase stability, thereby providing a good basis for analyzing frequency locking dynamics [14].

4. Synchronization stability and frequency locking dynamics. Lock time is one of the critical parameters in adaptive Gb/s networks [15]. The development was based on a compromise between bandwidth and stability margin to avoid ringing in the transient response [16]. The choice of a 45° phase margin was justified by the need to ensure monotonicity of the transient response [17]. To calculate the lock time, a model was developed including allowable frequency errors

Table 5

Loop filter parameters and measurement results

Parameter	Units	Meaning	Source/Note
ICP (Inductive Charge Pump Current)	mA	0.5	[13] High matching
Loop bandwidth	kHz	13	[13] Optimized
Filter capacity $C2/C3$	nF/pF	11.1/20	[13] Loop stability
Resistance $R2/R3$	kOhm	1.6/4.5	[13] Phase compensation
Phase Margin	deg.	45	[13] $\zeta \approx 0.707$

$$t_{settling} \approx \frac{1}{\zeta\omega_n} \ln\left(\frac{1}{error\sqrt{1-\zeta^2}}\right),$$

where $t_{settling}$ is the settling time and error is the relative frequency error [19]. The system's behavior was modeled using the MATLAB/Simulink programming environment on the MATLAB/C platform with the aid of the bilinear z-transform to emulate the continuous system behavior in the discrete domain. The results of the simulations corroborated the PLL stabilization time of 27.3 μs [19]. The use of the rotary frequency detector assured a locking range greater than 100 MHz, which along with the low jitter results confirms the high efficiency of the proposed architectural solutions.

Findings. *Efficacy of the TCXO as a monopole reference signal source*. In modern transceiver system architectures, temperature-compensated crystal oscillators (TCXOs) form a strategic basis to ensure long-term frequency stability under plesiochronous network operation conditions. The use of a TCXO as a single reference signal removes the problem of the accumulation of phase errors inherent in systems utilizing multiple local references, where frequency differences must be mitigated through the use of elastic buffers [1]. However, the high stability of the TCXO at small offsets is at odds with the necessity to ensure wideband jitter behavior during frequency division.

To ensure the optimization of the system's phase noise, the frequency division of the off-chip crystal oscillator (from 16.38 MHz to a reference value of 2.048 MHz [5]) must be accomplished with high accuracy, as the division directly defines the reference signal to the phase frequency detector (PFD). The mathematical model of the locking process is based on the computation of the natural frequency of the circuit (ω_n), which defines the bandwidth of the system response

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{2\pi\pi NC_1}}.$$

In this representation, K_{PD} stands for the phase detector gain, which is defined as the ratio of the charge pump current ICP and the phase error, with ICP possibly being 0.5 mA [7]. On the other hand, K_{VCO} refers to the slope of the VCO control signal, while N refers to the feedback loop division ratio [6]. A special role is assumed by capacitor C_1, which acts as a current integrator in the phase domain and places a pole at the origin to ensure a zero static phase error [9]. At the same time, an additional capacitance C_2 is needed to reduce high-frequency ripple on the VCO control signal, which is not reflected in the simplified equation for the value of ω_n.

Despite the presence of an ideal TCXO, the spectral purity of the signal is inevitably impaired during its passage through the active distribution networks.

Impact of distribution buffers and PCB layout on coherence. The physical layer of the clock distribution system is responsible for making a decisive contribution to the jitter budget. Nonlinear effects of the distribution buffers and PCB layout parameters convert deterministic jitter into phase errors, which impair coherence in networks with multiple nodes [3].

An important parameter is the offset voltage v_{offset} in the differential buffers, which shifts the threshold voltage V_{th} [13, 14]. This shift is responsible for duty cycle distortion, which is reflected in the appearance of high-frequency phase errors in the frequency domain [18]. At the PCB level, impedance inhomogeneities in connectors and vias result in reflections, which limit the eye diagram and the phase margin due to intersymbol interference (Table 6).

System Tradeoffs: Complexity, Accuracy, and Scalability. In designing the digital systems in deep submicron technologies, there is a need to transcend the traditional linear delay models, where the resistance and capacitance of the metal interconnects dominate the logic gate delay [20]. This calls for the use of wire load models and the iterative initial placement strategies to ensure the predictability of the synthesis process [21]. The choice between custom design, referred to as Full Custom, and standard cells, referred to as Standard Cell, is based on the scalability requirements. The use of standard cells and EDA tools reduces the time to market but requires the verification of the thermal noise impacts [10, 15]. The stability criterion is the root mean square value of the jitter ($\Delta t_{d.buff,rms}$) introduced by the active buffers

$$\Delta t_{d.buff,rms} = \sqrt{\frac{\zeta k T C_L}{I_{ss}^2}} .$$

In the above expression, k refers to the Boltzmann constant; T is the temperature; C_L is the capacitive load; I_{ss} is the differential pair tail current. The noise contribution factor ξ is defined as $(1 + av(2/3))$, where av refers to the cascade gain [9]. This expression reveals the basic trade-off: in order to minimize the RMS jitter, the I_{ss} current has to be increased exponentially, thereby increasing power consumption and cooling demands [4, 8, 22]. Verification of the above solutions involves comparing them with other possible synchronization approaches.

Comparative analysis: PLL, CDR, Distributed LO. In a synchronous network of considerable scale, it has been seen that a phase-locked loop (PLL) approach results in phase drift in the absence of a reference signal. This problem is addressed by employing a two-loop structure consisting of a clock-data recovery (CDR) component and a Clock-Jitter-Filter component, where the clock frequency is recovered from the data stream itself [16]. The main advantage of the above approach is the use of rotational frequency detectors. Rotary detectors are different from phase-frequency detectors (PFDs), as the former use the quadrature components of the clock signal to extract the frequency errors from random data, thereby allowing the system to operate over a wide range without any reference signal (Table 7) [17, 18].

The use of the LC VCO in the jitter filtering loop is critical to the reduction of the phase noise introduced by the primary recovery circuit [16]. This is necessary to achieve a high degree of coherence necessary for event detection systems such as high-energy physics and radar systems, where the timing of the data must remain in-

Table 6

Influence of distribution network parameters on signal quality

Parameter (Buffer/PCB)	Type of impact	Physical mechanism	Impact on jitter (RMS/P-P)	Minimization strategy
Differential cascade	Duty cycle distortion	Voltage offset (v_{offset})	Increase in P-P jitter	Slew Rate Increase (I_{ss}/C_L)
Line tracing	Reflections	Impedance mismatch	Deterministic jitter growth	Matching terminators with Z0 [14]
Via holes	Lane limitation	Parasitic inductance	Increase in ISI	Minimizing the number of transitions
Distribution buffer	Thermal noise	Carrier fluctuations	Increasing RMS jitter	Optimization of the I_{ss} tail current [4]
Connecting lines	Crosstalk	Electromagnetic communication	Periodic jitter	Differential shielding

The table depicts the relationship between the parameters of the physical layer and the degradation mechanisms for the signal, where the control of the signal slew rate is the major method for the mitigation of the phase shift. The trade-offs involving complexity and accuracy are further seen when moving to submicron process technologies, where interconnect delays dominate

Table 7

Comparison of synthesis and frequency distribution architectures

Architecture	Power consumption, mW	RMS jitter, ps	Local reference	Scope of application
Precision PLL [7]	36	3.3	Required	Local synthesis of LO
Standard CDR	80	4.6–5.2	Not required	Data receivers
Distributed LO [9]	170	8.0–15	Backbone network	Distributed systems
2-Loop CDR (Proposed) [9]	170	4.2	Not required	Synchronous readout networks
Fractional-N PLL	55	6.0–10	Required	Fine-pitch frequency grids

Analysis shows that the proposed architecture results in battery longevity with the power consumption of 170 mW being justified as the RMS jitter of 4.2 ps is attained even when the input ISI is as high as 150 ps [9, 19]

variant to delays introduced in the communication channel [23, 24].

Conclusions.

1. Introduction to phase coherence in multichannel systems. In the context of modern wireless communication systems such as Massive MIMO systems and software-defined radio systems, the concept of phase coherence is critical to the successful implementation of spatial multiplexing as well as beamforming techniques. However, the achievement of strict time synchronization at gigahertz-scale frequencies is hampered by the issue of phase noise as well as timing jitter. In wideband systems, timing jitter is considered a critical hindrance to the growth of the radio channel throughput, as jitter directly impacts the system's dynamic range as well as the bit error rate (BER).

In the context of decentralized systems functioning in plesiochronous mode, the issue of phase drift as well as frequency differences between different system nodes is unavoidable, thereby necessitating the use of sophisticated compensation algorithms as well as buffering techniques. Signal degradation over time is a critical issue faced by such systems, thereby impacting the concept of phase coherence. A strategic way to overcome the aforementioned issues is to implement a centralized reference oscillator system with correlated phase noise as well as minimal timing skew.

2. Centralized reference oscillator architecture and frequency synthesis. The proposed system utilizes a precision PLL frequency synthesizer architecture, which is realized using a common source configuration for multiple RF paths. The PLL feedback loop includes a phase frequency detector (PFD), a charge pump (CP), a voltage-controlled oscillator (VCO), and a high-speed downconversion circuit. The utilization of a single VCO ensures that the phase variations of the reference signal are the same for both transmitters, a necessary condition for the transmitter coherence. In the feedback loop, a combined divider circuit is used, allowing flexibility in tuning the frequency within the 1.17–1.18 GHz range. Mathematically, the division ratio is defined as $N = 16M + A$, where M is the program counter (Counter-M), and A is the absorption counter (Counter-A/Swallow Counter). The utilization of a dual-module prescaler (DMP) with a 16/17 ratio, along with true single-phase clocking (TSPC) logic, enables the achievement of high spectral purity with significantly lower power consumption. This flexibility of the frequency grid is a necessary condition for SDR systems that need to operate with a variety of communication systems.

3. Low jitter design: charge pump and dividers. Significant reduction in RMS jitter is achieved by optimizing the values of the most important components in the PLL circuit. The prescaler circuit makes extensive use of a source-coupled logic (SCL) architecture along with high-performance D-type flip-flops. Unlike conventional methods, the tail current source is completely eliminated in the proposed architecture. This results in a significant increase in the speed of the output stages. In addition, the direct implementation of OR logic within the flip-flop structure eliminates signal propagation delays. This is because the complexity of the digital logic is a direct cause of jitter. Therefore, the implementation of OR logic results in a direct reduction in the jitter phenomenon. Significant emphasis has been laid on the optimization of the currents in the charge pump. In conventional PLL architectures, the dispersion in the pump and leakage currents is the primary cause of the appearance of spurious spikes. In the proposed PLL architecture, an innovative charge pump architecture is implemented. This architecture makes extensive use of an operational error amplifier to ensure the precise matching of the VX and VOUT nodes. In addition, the implementation of a self-biasing cascode current mirror ensures the precise matching of the currents I1 and I4. The stability of the currents in the CP is constant over a wide range of control voltage values. This ensures the high temporal stability of the PLL architecture.

4. Results analysis: achieving phase coherence and temporal stability. The experimental verification of the system, which was fabricated using 0.18-μm CMOS technology, demonstrated the achievement of precision characteristics. The root mean square jitter value was found to be 3.3 ps (RMS). In addition, the spectral analysis of the output signal at a frequency of 1.173 GHz indicated a phase noise level of –101.52 dBc/Hz at a frequency offset of 100 kHz. This low level of noise is critical when the signal is in close proximity to the carrier, especially in the context of achieving minimum interchannel interference in orthogonal frequency division multiplexing systems, wherein a high level of subcarrier density is required. In the context of the system's power efficiency, the value of 36 mW at a supply voltage of 1.8 V is considered optimal for the design of multichannel RFIC systems. In addition, the frequency lock time of 27.3 microseconds ensures a high level of dynamic stability when the channel is being switched. Thus, it is evident that the proposed frequency division and current stabilization node topology effectively suppress the PLL noise generated internally.

5. Practical value for MIMO, SDR, and coherent systems. The proposed architecture is of utmost significance in the development of SDR technology, which demands the provision of a coherent clocking solution devoid of the need for bulky external filtering. In this context, the RMS jitter of 3.3 ps is a significant improvement that finds practical application in the improvement of the error vector magnitude (EVM), thus allowing for the stable deployment of higher-order quadrature modulation schemes, including 256 QAM. In the context of coherent systems, the proposed solution finds practical application in the reduction of the burden of the digital processing system, which would otherwise be required to implement computationally intensive software-based phase skew correction algorithms.

In the context of massive MIMO systems, the proposed solution finds practical application in the economies of scale that it provides through the synchronization of hundreds of antenna elements. In this context, the low power consumption per node (36 mW) is a major advantage of the proposed solution, which finds practical application in the improvement of the efficiency of the beamforming process. This, in turn, improves the efficiency of the radio link, thus allowing for the extension of the network coverage. In this context, the proposed system finds practical application as a highly

efficient hardware solution for the next generation of wireless communication systems.

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References.

1. Wojciechowski, A. A., Marcinek, K., & Pleskacz, W. A. (2023). Relative Jitter Measurement Methodology and Comparison of Clocking Resources Jitter in Artix 7 FPGA. *Electronics*, 2023, 4297. https://doi.org/10.3390/electronics12204297

2. Challagundla, D., Sundarapu, V. K., Bezzam, I., & Islam, R. (2025). *TSPC-PFD: TSPC-Based Low-Power High-Resolution CMOS Phase Frequency Detector*. arXiv.2508.16933. https://doi.org/10.48550/arXiv.2508.16933

3. Jiang, Y., Yu, Y., Tang, L., Yang, J., Lu, Y., & Yu, Z. (2023). A Low Jitter, Wideband Clock Generator for Multi-Protocol Data Communications Applications. *Electronics, 12*, 3196. https://doi.org/10.3390/electronics12143196

4. Clark, K. A., Zhou, Z., & Liu, Z. (2024). Clock synchronizing radio access networks to picosecond precision using optical clock distribution and clock phase caching. *Journal of Optical Communications and Networking*, *16*(1), 89-97. https://doi.org/10.1364/JOCN.500459

5. Ghahramani, M., Rajavi, Y., Khalili, A., & Kavousian, A. (2016) *Apparatus and method for quadrupling frequency of reference clock*. (US Patent App. 14/605,734).

6. Pan, Ch., Shi, Ch., Zhao, G., Liu, B., Huang, L., & Zhang, R. (2022). A 21.3–24.5 Gb/s low jitter PLL-based clock and data recovery circuit with cascode-coupled quadrature LC-VCO. *IEICE Electronics Express*, *19*(24), 1-6. https://doi.org/10.1587/elex.19.20220432

7. Lu, T., Zhigong, W., Hong, X., Xiaohu, H., Yong, X., & Ling, S. (2010). A low-jitter RF PLL frequency synthesizer with high-speed mixed-signal down-scaling circuits. *Journal of Semiconductors*, *31*(5). https://doi.org/10.1088/1674-4926/31/5/055008

8. Analog Devices (2018). *LTC6952: Ultralow jitter, 4.5GHz PLL with 11 outputs and JESD204B/C support* (Rev. A). Mouser Electronics. https://www.mouser.com/pdfdocs/ltc6952.pdf

9. Tontisirin, S., & Tielert, R. (2007). Gb/s CDR circuit for large synchronous networks. *ESSCIRC 2007 – 33rd European Solid-State Circuits Conference*, (pp. 528-531). Munich, Germany. https://doi.org/10.1109/ESSCIRC.2007.4430358

10. Zhou, Z., Nopchinda, D., Darwazeh, I., & Liu, Z. (2023). Synchronising Clock and Carrier Frequencies with Low and Coherent Phase Noise for 6G. *2023 IEEE Radio and Wireless Symposium (RWS)*. https://doi.org/10.1109/RWS55624.2023.10046337

11. Zuo, S., Zhao, J., & Zhou, Y. (2021). A 0.8 V, 5.3–5.9 GHz Sub-Sampling PLL with 196.5 fs_{rms} Integrated Jitter and −251.6 dB FoM. *Sensors*, *21*, 7648. https://doi.org/10.3390/s21227648

12. Liu, T. (2022). *A 4.9-GHz Low Power, Low Jitter, LC Phase Locked Loop*. arXiv.2202.05730. https://doi.org/10.48550/arXiv.2202.05730

13. Ray, Yu., & Ghosh, A. (2024). *A 0.03mm2 100-250MHz Charge-Pump or Amplifier-Less Integrating Sub-Sampling PLL for Ultra-low Power Communication and Computing*. arXiv.2410.16310. https://doi.org/10.48550/arXiv.2410.16310

14. Calvet, D. (2020). Clock-centric Serial Links for the Synchronization of Distributed Readout Systems. *IEEE 22nd Real Time Conference*, 67(8), 1912-1919. https://doi.org/10.48550/arXiv.2010.14164

15. Xiao, H., Houpeng, Ch., Zhitang, S., Daolin, C., & Xi, L. (2013). A low jitter PLL clock used for phase change memory. *Journal of Semiconductors*, *34*(2), 025012. https://doi.org/10.1088/1674-4926/34/2/025012

16. Thool, P., Dhande, J. D., & Sadawarte, Y. A. (2022). A Review on Design and Analysis of Low Power PLL for Digital Applications and Multiple Clocking Circuits. *International Journal for Research in Applied Science & Engineering Technology (IJRASET)*, *10*(IV), 178-182. https://doi.org/10.22214/ijraset.2022.41193

17. Clark, K. A., Htay, Z., Zhou, Z., Kassem, A., Pertoldi, A., Rudin, B., Emaury, F., Darwazeh, I., & Liu, Zx. (2025). *Synchronous Clock and RF Carrier Transmission for Radio Access Network Fronthaul*. *arXiv.2506.05811*. https://doi.org/10.48550/arXiv.2506.05811

18. Pearson, C. (2015). 1.4GHz Low Jitter PLL with Clock Distribution Solves Difficult Clocking Problems: Multi-Clock Synchronization and Data Converter Clocking. *LT Journal of Analog Innovation*, 17-23. https://www.analog.com/en/resources/technical-articles/low-jitter-pll-with-clock-distribution-solves-difficult-clocking-problems.html

19. Ashari, Z. M., & Nordin, A.N. (2012). Theoretical modeling and simulation of phase–locked loop (PLL) for clock data recovery (CDR). *IIUM Engineering Journal*, *12*(5). https://doi.org/10.31436/iiumej.v12i5.250

20. Yevseiev, S., Kuznietsov, O., Biesova, O., Kyrychenko, D., Lukashuk, O., Milevskyi, S., ..., & Sobchenko, V. (2021). Development of a method for estimating the effect of transformation of the normalized frequency mismatch function of a coherent bundle of radio pulses on the quality of radar frequency resolution. *Eastern-European Journal of Enterprise Technologies, 4*(4(112)), 13-22. https://doi.org/10.15587/1729-4061.2021.238155

21. Shevchenko, V., Syvytsky, Y., Derevianko, Y., Bakaiev, O., Korol, O., Pohasii, S., ..., & Komar, O. (2025). Development of a model of the useful effect of the system at different levels of subsystem interchangeability in the problem of optimizing the allocation of a limited resource. *Eastern-European Journal of Enterprise Technologies, 5*(4(137)), 64-75. https://doi.org/10.15587/1729-4061.2025.342299

22. Pohasii, S., Holdobin, S., Brynza, N., Vilkhivska, O., Bilotserkivskyi, O., & Samorodov, B. (2024). Management Models for Wireless Communication Channel Interference Monitoring. *2024 8th International Symposium on Multidisciplinary Studies and Innovative Technologies (ISMSIT)*, Ankara, Turkiye, 1-7. https://doi.org/10.1109/ISMSIT63511.2024.10757190

23. Yevseiev, S., Milov, O., Milevskyi, S., Voitko, O., Kasianenko, M., Melenti, Y., Pohasii, S., ..., & Faraon, S. (2020). Development and analysis of game-theoretical models of security systems agents interaction. *Eastern-European Journal of Enterprise Technologies, 2*(4(104)), 15-29. https://doi.org/10.15587/1729-4061.2020.201418

24. Herasymov, S., Olenchenko, V., Yevseiev, S., Milevskyi, S., & Pohasii, S. (2022). Investigation of the Dynamic Filters' Characteristics for the Analysis of Random Signals During Data Transmission. *2022 IEEE 3rd KhPI Week on Advanced Technology (KhPIWeek)*, Kharkiv, Ukraine, 1-6. https://doi.org/110.1109/KhPIWeek57572.2022.9916327

Синхронізація на основі опорного сигналу з низьким джиттером для двох радіочастотних передавачів

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Мета. Розробка блоку синхронізації з низьким джиттером для двох радіопередавачів на основі спільного опорного генератора, виконаного за CMOS-технологією з розподільчою здатністю 0,18 мкм.

Методика. У роботі використані методи схемотехнічного моделювання в середовищі MATLAB/Simulink із використанням білінійного *z*-перетворення для аналізу динаміки петель ФАПЧ. Проєктування топології друкованої плати здійснювалося з урахуванням електродинамічних параметрів (імпеданс 50 Ом, матеріал FR-4) й екстракції RC-параметрів для мінімізації фазової неузгодженості. Експериментальна перевірка проводилася на базі КМОН-технології 0,18 мкм.

Результати. Створена двопетльова архітектура (блок відновлення тактової частоти CDR і фільтр джитера), що забезпечує стабільність сигналу на

частоті 1,173 ГГц. Досягнуто рівня фазового шуму –101,52 дБс/Гц при відстрочці 100 кГц і середньоквадратичного джитера (RMS) 3,3 пс для синтезатора та 4,2 пс для вузла CDR. Час захоплення частоти становить 27,3 мкс при споживаній потужності 36 мВт на один вузол.

Наукова новизна. Обґрунтовано використання інноваційної архітектури зарядного насоса (charge pump) з операційним підсилювачем помилки для прецизійного вирівнювання потенціалів вузлів, що мінімізує паразитичні шпори й фазовий зсув. Уперше запропоновано інтеграцію логіки "АБО" безпосередньо в структуру D-тригерів прескалера, що усуває додаткові затримки поширення сигналу та знижує кумулятивний джитер.

Практична значимість. Запропоноване рішення дозволяє відмовитися від складних програмних алгоритмів корекції фазового зсуву в системах Massive MIMO та SDR. Низький рівень джитера (3,3 пс) дає змогу стабільно використовувати високорівневі схеми квадратурної модуляції (до 256 QAM), покращуючи показник модуляційної помилки (EVM) й ефективність радіоканалів наступного покоління.

Ключові слова: *фазова когерентність, джиттер, PLL, CDR, TCXO, попередній дільник, синхронізація, формування променю*